CLAIMS

1. A method for transferring a plurality of bits from a source register to a destination register, comprising the steps of:

loading the source register with the plurality of bits;

dividing the source register into a plurality of first level subsets;

identifying the bits in each subset which are to be transferred to the destination register, wherein the subsets each have a number of transfer data bits and non-transfer data bits;

aligning the transfer data bits in each first level subset to a first side thereof to form corresponding second level subsets of the transfer data bits;

loading the transfer data bits from the second level subsets into the destination register aligned to the first side of the destination register.

2. The method of claim 1 further comprising combining pairs of the first level subsets, each pair comprising a first of the pair and a second of the pair, by level shifting the transfer data bits of the first of the pairs and combining the level-shifted transfer bits with the second of the pairs.

3. The method of claim 2, wherein the step of combining pairs is further characterized as level-shifting the transfer bits of the pairs by an amount equal to the number of non-transfer bits of the first level subset which corresponds to the second of the pair.

4. The method of claim 3, wherein the step of aligning is further characterized as aligning the transfer bits in a logic order.

5. The method of claim 4, wherein the step of combining is further characterized as combing the transfer bits in the logic order.

6. The method of claim 1, wherein the number of non-transfer bits for at least one of the subsets is zero.

7. A method for manipulating a plurality of bits from a source register to a destination register, comprising the steps of:

loading the source register with the plurality of bits;

dividing the source register into a plurality of first level subsets;

identifying the bits in each subset which are to be transferred to the destination register, wherein the subsets are in logic order and each have transfer data and non-transfer data;

aligning the transfer data in each first level subset to a first side thereof to form second level subsets in logic order;

forming first adjoining pairs of second level subsets each having a second level subset on the first side and a second level subset on a second side;

combining the first adjoining pairs by shifting the data of each of the second level subsets on the second side to the first side by an amount equal to the number of non-transfer bits in the second level subset on the first side to form third level subsets;

forming second adjoining pairs of third level subsets each having a third level subset on the first side and a third level subset on the second side;

combining the second adjoining pairs by shifting the data of each of the third level subsets on the second side to the first side by an amount equal to the number of non-transfer bits in the third level subset on the first side to form fourth level subsets;

loading the transfer data from the fourth level subsets into the destination register in consecutive order aligned to the first side of the destination register.

8. A circuit comprising:

a source register with the plurality of bits divided into a plurality of first level subsets;

means for identifying the bits in each subset which are transfer bits and non-transfer bits;

arranger means for aligning the transfer data bits in each first level subset to a first side thereof to form corresponding second level subsets of the transfer data bits;

a destination register; and

coupling means for loading the transfer data bits from the second level subsets into the destination register aligned to the first side of the destination register.

9. The circuit of claim 8 further comprising a combiner means for combining pairs of the second level subsets, each pair comprising a first of the pair and a

second of the pair, by shifting the transfer data bits of the first of the pairs to form shifted transfer bits and combining said shifted transfer bits with the second of the pairs.

10. The circuit of claim 9, wherein the arranger means comprises a plurality of arrangers each for a receiving a set of mask bits, each set of mask bits corresponding to one of the arrangers, each arranger corresponding to a subset of the first level subsets, each arranger comprising:

a first multiplexer having a first input coupled to receive a first bit from the subset of the first level subsets to which the arranger corresponds, a second input coupled to receive a second bit from the subset of the first level subsets to which the arranger corresponds, a control input for receiving a first mask bit from the set of mask bits to which the arranger corresponds, and an output;

a second multiplexer having a first input to receive the first bit, a second input coupled to the output of the first multiplexer, a control input for receiving a second mask bit from the set of mask bits to which the arranger corresponds, and an output;

a third multiplexer having a first input coupled to the output of the first multiplexer, a second input coupled a third bit from the subset of the first level subsets to which the arranger corresponds, a control input for receiving the second mask bit, and an output;

a fourth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled a fourth bit from the subset of the first level subsets to which the arranger corresponds, a control input for receiving a third mask bit from the set of mask bits to

which the arranger corresponds, and an output as a first output of the arranger;

a fifth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled to the output of the second multiplexer, a control input for receiving the third mask bit, and an output as a second output of the arranger; and

a sixth multiplexer having a first input coupled to the output of the second multiplexer, a second input coupled to receive the first bit, a control input for receiving the third mask bit, and an output as a third output of the arranger.

11. The circuit of claim 9, wherein each combiner means comprises:

a first plurality of multiplexers coupled to the first of the pair and a first mask signal;

a second plurality of multiplexers coupled to the first plurality of multiplexers and a second mask signal; and

a third plurality of multiplexers coupled to the second plurality of multiplexers and a third mask signal.

12. A circuit, comprising:

a source register having a plurality of bits and for containing transfer and non-transfer data contained in first and second subsets of the plurality of bits;

a destination register;

a first arrangement means coupled to the first subset for placing the transfer bits contained in the first subset on a first side of the first arrangement means;

a second arrangement means coupled to the second subset for placing the transfer bits contained in the second subset on the first side of the first arrangement means;

shifter/combiner means for shifting the data in the second arrangement means toward the first side of the shifter/combiner means by an amount equal to the number of non-transfer bits in the first subset; and

coupling means for coupling the contents of the first and second means into the destination register.

13. The circuit of claim 12, wherein the coupling means is further characterized as coupling the contents of the first and second means into the first side of the destination register.

14. The circuit of 12,wherein the first arrangement means comprises:

a first multiplexer having a first input coupled to receive a first bit from the first subset, a second input coupled to receive a second bit from the first subset, a control input for receiving a first mask bit, and an output;

a second multiplexer having a first input to receive the first bit, a second input coupled to the output of the first multiplexer, a control input for receiving a second mask bit, and an output;

a third multiplexer having a first input coupled to the output of the first multiplexer, a second input coupled a third bit from the first subset, a control input for receiving the second mask bit, and an output;

a fourth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled a fourth bit from the first subset, a control input for receiving a third mask, and an output as a first output of the first arrangement means;

a fifth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled to the output of the second multiplexer, a control input for receiving the third mask bit, and an output as a second output of the arrangement means; and

a sixth multiplexer having a first input coupled to the output of the second multiplexer, a second input coupled to receive the first bit, a control input for receiving the third mask bit, and an output as a third output of the arrangement means.

15. The circuit of claim 12, wherein the shifter/combiner means comprises:

a first plurality of multiplexers coupled to the second arrangement means and a first mask signal;

a second plurality of multiplexers coupled to the first plurality of multiplexers and a second mask signal; and

a third plurality of multiplexers coupled to the second plurality of multiplexers and a third mask signal.